Implementation of AMBA-APB Protocol with Low Power Dissipation

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Abstract: The aim of the dissertation is to put in force AMBA-APB(Advance Microcontroller Bus Architecture-Advance Peripheral Bus) Bridge for low power dissipation. For this, simulation and synthesis of the complex bridge interface is designed which could offer minimum electrical power strength consumption and high frequency band width among AMBA high performance or speedy or high velocity buses like ASB and low active APB buses. For designing any type of ic three main criteria's are speed ,power and area. Clock is a first-rate situation in designing of any digital sequential gadget. Clock skew is generated when the distinction in clock signal arriving time between two adjacent register. One of the strategies to limit clock skew is master slave flip-flop. So in this dissertation work we used flip-flop as a memory element with master slave concept which is based on the finite state machine. Advanced Peripheral Bridge with clock skew reduction technique is enforced within the thesis the usage of verilog HDL. For the simulation and synthesis motive, design usage summary and power details Xilinx's-ISE design suite, model 14.1 has been used. Power record is added for developing better know-how of the energy utilization in any gadget. The power document offers the electricity consumption precise. Hence, the whole clocks energy intake is of 0.35 mW, general hierarchy strength consumption of 0.13 mW and general on chip logical strength consumption of 0.040 W had been extracted from Xilinx X-Power analyzer device when APB Bridge is designed beneath the proposed design technique.

Keywords: AMBA, AHB, APB, Soc(System on Chip), Clock Skew, FSM.

Introduction

Basically system on chip style numerous elements of computer or different electronic system are mounted onto one chip. A widely known on chip buses are referred to as advanced microcontroller bus architecture plays an important role in system on chip. AMBA conception is introduced initial time by ARM therefore it's a registered of ARM Ltd. one in every of the appliance of AMBA buses is fashionable transportable mobile devices like (Smartphone, hard Disk) during which a variety of application specific integrated circuits (ASIC) and system on chip (SOC) with its application processors are used. Additionally AMBA style Specification provides a platform to the designer that is sort of freelance to technology and therefore the technique organizes the varied peripherals like UART, Keypads, and PIO in SOC style. AMBA specification provides a typical for interaction and communication. Advanced Microcontroller Bus design (AMBA) specification defines an on chip communication commonplace for planning high performance embedded microcontroller processors or systems. Advanced Microcontroller Bus design specifications offer technology freelance resolution for communication between master and its slaves.

Literature Survey

In 2015 IEEE Kiran Rawat et al. [5] presented an article. In this article presented, the main challenge for a style engineer isn't only to style a flourishing SoC with a well-structured and synthesizable RTL code but also to style it with economical in energy and optimized in power consumption. The aim of the paper is to implement AMBA APB (advanced microcontroller bus architecture - advanced peripheral bus) Bridge with economical preparation of system resources. For this, simulation and synthetization of the advanced bridge interface is meant which may offer minimum power consumption and low information measure between AMBA high speed ASB and low speed APB buses. Clock could be a major concern in planning of any digital consecutive system. Clock skew is introduced when the distinction is generated between the arrival times of clock signal. One of the approaches to reduce clock skew is ripple counter. One will use 3 bit up or down ripple counter approach. APB Bridge with clock skew diminution technique is enforced within the paper using Verilog HDL. For the simulation

purpose, Model-Sim Version 10.3 has been used. For the synthetization purpose, style utilization outline and power details Xilinx-ISE style suite, version 13.4 has been used. Power report is introduced for developing higher understanding of the facility utilization in any system. The facility report offers the facility consumption outline. Hence, the entire clocks power consumption is of 0.39 mW, total hierarchy power consumption of zero.57 m Wand total on chip logical power consumption of 0.113 W are extracted from Xilinx X-Power analyzer tool when APB Bridge is styled or meant or intended underneath the planned design approach.

In 2014 IEEE Pranav Kumar et al. [6] proposed a paper. In this paper proposed, verifying a posh SOC is difficult. The test bench and test cases should be developed early as these are used for everything from SOC verification to realize higher coverage on feature protocol coverage, if integration and performance verification. Time to plug makes early computer code development a necessity. Verification power-assisted with early computer code development wants quite dynamic simulation and emulation methodology involves rescue. Firstly, the verification of RTL in system atmosphere has been economical with SV/UVM methodologies that specialize in reprocess on test bench and test cases beside the verification atmosphere around Verification information science.

In 2015 IEEE Jasmine Chhikara et al. [7] proposed an article. In this proposed article, all style units incorporate smaller practical blocks referred to as scheme or module. For effective functioning of the system these modules need to be in set with one another and share resources. Downside starts when one module follows totally different or completely different protocol as others and every module has its different bit rate or baud rate of data transfer which may be either asynchronous or synchronous. The paper takes an example of I2C protocol and AMBA APB protocol to explain the design that defines how knowledge is transferred from one protocol to a different. It exploits the versatile protocols of I2C to form it compatible with APB protocol.

Problem Statement

In this brief, we have done the survey of different on-chip protocols along with their features and architectures. A descriptive comparison between various on-chip protocols is needed. So we have to find out the efficient protocol as it can efficiently transfers block of data thereby reducing the hardware resources and minimal power consumption. This can be verified by implementing the our projected protocol at RTL in HDL and comparing the same with other protocols by considering various parameters such as transfer time consumption, wire efficiency, valid data bandwidth, dynamic energy efficiency and power consumption.

Proposed Methodolgy

The main difficulty facet by the design or layout design engineer to design the successful SOC with well-structured and synthesizable RTL code are power consumption and clock skew. The aim of this paper is to formulate the problem in design of successful SOC and propose a general mechanism steps to solve this problem of power consumption. Mainly in digital sequence circuit clock is major concern. To minimize the clock skew problem we use flip-flop master slave approach and reduce the total power consumption in SOC. General Steps or proposed methodology steps are given below:

1. Identify the clock signal.
2. Transition of clock signal.
3. Examined each and every clock precisely.
4. Find interrelation and unused clock
5. Design state diagram.
6. Behavioral description.
7. RTL synthesis.
8. Simulation
9. Power analysis.

Simulation Results

For implementation purpose of AMBA(Advanced Microcontroller Bus Architecture) APB(Advanced Peripheral Bus) Bridge with its various blocks like master-slave flip flop, state machine, project decoder and other blocks Verilog Hardware Description Language is used. Simulation has done by using Xilinx ISE Design Suite version 14.1. This will generate waveform in different phenomenon. Xilinx is also used for the logic synthesis and extraction of design utilization summary.

Figure2. RTL Technology View of AMBA-APB

Power Analysis

Table 1 Power Report Analysis between Proposed and Previous Methodology

	Total Clock domain	Total Hierarchy power	Total On chip power	Frequency(MHz)
Power Report of APB bridge with reset controller and three bit ripple down counter approach(W)	0.00039	0.00057	0.113	50
Power Report of APB bridge with efficient system resource approach(W)	0.00035	0.00013	0.040	50

Table No. 1, represents that only total clock domain power of 0.35 mW, total hierarchy power of 0.13 mW and total on chip power of 0.040 W are consumed by the proposed design approach. The difference between the power factors has been observed when flip-flop with master slave condition approach is implemented over the AMBA APB Bridge.

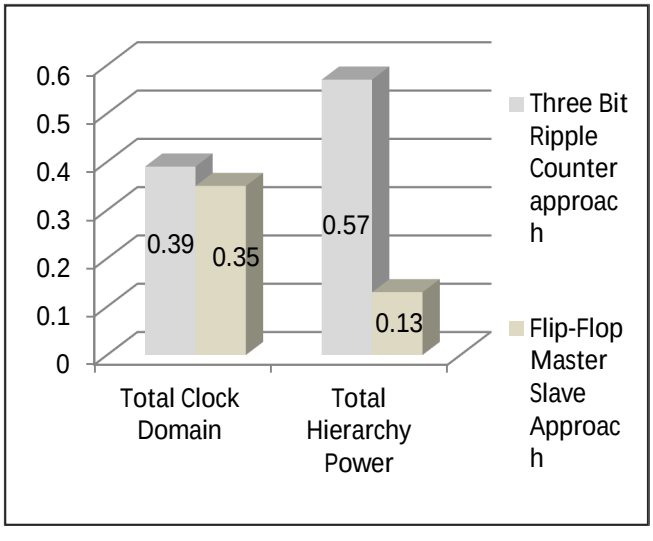

Figure2. Comparison Chart between Previous and Proposed Methodology in term of Power Consumption in mW

As we can see from the figure 2 the comparison chart between previous methodology (Three bit Ripple Counter Approach) and proposed methodology (Flip-Flop Master-Slave Approach) in term of total clock domain and total hierarchy power consumption in mW.

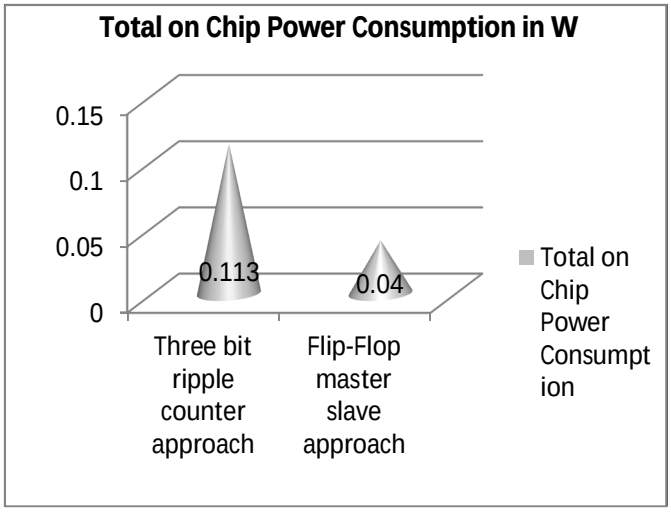

Figure3. Comparison Chart between Previous and Proposed Methodology in term of Total on Chip Power Consumption in W

As we can see from the figure 3 the comparison chart between previous methodology (Three bit Ripple Counter Approach) and proposed methodology (Flip-Flop Master-Slave Approach) in term of Total on Chip Power Consumption in W.

Conclusion

In this paper the designing of AMBA(Advanced Microcontroller Bus Architecture) APB(Advanced Peripheral Bus) Bridge has done by using Verilog Hardware Descriptive Language with memory element master slave flip flop which is based on finite state machine. The objective of the thesis became to design an APB bridge with green device sources approach for minimizing the clock skew. Also strength reports are included with the proposed layout. For simulation purpose Xilinx ISE Design Suite version Xilinx 14.1 has used and also used for synthesis. For Power simulation purpose Xilinx X-Power analyzer tool has been used. Clock frequency for APB simulation has taken 50 MHz.

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